## IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

***Listing of Claims:***

1. (Currently amended) A processor, comprising:

at least one register file;

at least one execution unit coupled to the at least one register file, the at least one register file being available to programs for temporarily storing operands and results;

at least one bypass circuit operatively coupled to said at least one register file and said at least one execution unit, said at least one bypass circuit capable of arbitrating access by said at least one execution unit to said at least one register file; and

a backing register file operatively coupled to said at least one register file, ~~and where~~ said backing register file [[is]] being ~~operationally and responsively coupled to at least one user-visible instruction, the user-visible instruction having registering windowing capability or having the capability to use the backing register file in a native mode, wherein the native mode is the capability to address each register of the backing register file by way of addresses or at random~~ inaccessible to the at least one execution unit and, in at least one mode, is always visible outside the processor and available to the programs at any privilege level.

2. (Currently amended) The processor of claim 1, ~~further comprising~~ wherein the at least one register file comprises a plurality of register files, the ~~and further comprising~~ at least one execution unit being operably connected to each register file of said plurality of register files, and where said backing register file is operably connected to each register file of said plurality of register files ~~providing~~ thereby ~~the ability to~~ allowing a transfer of values from any designated location in any designated register file of said plurality of register files to any designated location in said backing register file, and from any designated location in said backing register file to any designated location in any designated register file of said plurality of register files.

3. (Currently amended) The processor of claim 1, further comprising a connection circuit having a first connection and a second connection, where said first connection is operably connected to said backing register file from the at least one register file and said second connection is operably connected to a main memory from the said backing register file, the connection circuit placing the backing register file in communication with the main memory.

4-18. (Canceled)

19. (New) The processor of claim 1, the at least one mode comprising a native mode in which every register in the backing register file is addressable by a unique address.

20. (New) The processor of claim 19 wherein the backing register file is further operable in a windowing mode wherein the backing register file mimics register windowing functionality wherein less than all the registers in the backing register file is accessible to a particular process at one time.

21. (New) The processor of claim 20 wherein the backing register file operates in one of the windowing mode or the native mode depending upon instructions in a current instruction stream of a current process, wherein when the instruction stream includes register windowing instructions, the backing register file operates in the windowing mode, and when the instruction stream does not include register windowing instructions then the backing register file operates in the native mode.